REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-7, 9-18, 20-32 and 34-41 were pending. Claims 1-7, 9-18, 20-32 and 34-41 have been rejected.

Claims 1, 12, and 26 have been amended. No claims have been cancelled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38 and 40-41 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,282,556 to Chehrazi, et al. ("Chehrazi") in view of U.S. Patent No. 6,036,350 to Mennemeir, et al. ("Mennemeir").

Applicants have amended claim 1 to include selecting a first plurality of numbers from the first vector and a second plurality of numbers from the second vector according to a configuration specified by the instruction.

Chehrazi discloses the sum of absolute differences (SABD) instruction. More specifically, Chehrazi discloses:

> FIG. 20B is a diagram 570 that illustrates the operation of the SABD instruction in one exemplary mode. Input register 310 contains 16 separate 8-bit operands called 310(a)-310(p). Input register 312 contains 16 separate 8-bit operands called 312(a)-312(p). As shown in FIG. 20B, each separate operand of register 310 has a corresponding operand of register 312, e.g., operand 310(f) corresponds to operand 312(f), etc. The data path circuit 300 first uses one of its 16 8-bit subtractor circuits, 322 or 324 (FIG. 4), to perform subtraction on each corresponding operand pair, specifically subtracting Vs from Vt. The other 16 8-bit subtractor circuit then performs the same subtraction in parallel but between Vt from Vs. This simultaneously products 32 separate differences and a positive and a negative difference for each corresponding operand pair. Multiplexers in circuit 332 then select the positive difference for each operand pair as

> the absolute value difference for each pair. These absolute value differences are them summed together at 575 of FIG. 20B to arrive at a single result sum stored in register 415.

(Chehrazi, col. 20, line 61-col. 21, line 12) (emphasis added)

Thus, Chehrazi merely discloses that each operand in one register has a corresponding operand in another register. In contrast, amended claim 1 refers to selecting a first plurality of numbers from the first vector and a second plurality of numbers from the second vector according to a configuration specified by the instruction.

Mennemeir discloses a technique for sorting signed packed numbers of two operands (Abstract), and similarly to Chehrazi fails to disclose selecting a first plurality of numbers from the first vector and a second plurality of numbers from the second vector according to a configuration specified by the instruction, as recited in amended claim 1.

It is respectfully submitted that Chehrazi does not teach or suggest a combination with Mennemeir, and Mennemeir does not teach or suggest a combination with Chehrazi. Chehrazi teaches pipelining for a media processor. Mennemeir, in contrast, teaches sorting signed packed numbers. It would be impermissible hindsight, based on Applicants' own disclosure, to combine Chehrazi and Mennemeir.

Furthermore, even if Chehrazi and Mennemeier were combined, such a combination would lack selecting a first plurality of numbers from the first vector and a second plurality of numbers from the second vector according to a configuration specified by the instruction, as recited in amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under U.S.C. § 103(a) over Chehrazi in view of Mennemeier.

Given that amended claims 12 and 26, and claims 2-3, 5-7, 9-11, 13-14, 16-18, 20-22, 27-28, 30-32, 34-38 contain related limitations, Applicants respectfully submit that claims

amended claims 12 and 26, and claims 2-3, 5-7, 9-11, 13-14, 16-18, 20-22, 27-28, 30-32, 34-38 are not obvious under U.S.C. § 103(a) over Chehrazi in view of Mennemeier.

Claim 23 includes a selector circuit configured to select a first plurality of numbers from the first vector and a second plurality of numbers from the second vector.

As set forth above, Chehrazi discloses two subtractor circuits, and a multiplexer circuit (Figure 4, col. 21, lines 1-10). In contrast, claim 23 refers to a selector circuit configured to select a first plurality of numbers from the first vector and a second plurality of numbers from the second vector.

As set forth above, Mennemeier, similarly to Chehrazi, fails to disclose such limitations of claim 23.

Thus, neither Chehrazi, Mennemeir, nor a combination thereof, discloses a selector circuit configured to select a first plurality of numbers from the first vector and a second plurality of numbers from the second vector, as recited in claim 23.

Therefore, Applicants respectfully submit that claim 23 is not obvious under U.S.C. § 103(a) over Chehrazi in view of Mennemeier.

Given that claims 25, 24, 40, and 41 contain related limitations, Applicants respectfully submit that claims 25, 24, 40, and 41 are not obvious under U.S.C. § 103(a) over Chehrazi in view of Mennemeier.

Claims 4, 15, 29 and 39 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Chehrazi, in view of Mennemeier, as applied to claims 1, 2, 12, 26 and 27 above, and further in view of EP App. No. 0485776A2 to Diefendorff, et al. ("Diefendorff").

It is respectfully submitted that Chehrazi does not teach or suggest a combination with Mennemeier and Diefendorff, Mennemeier does not teach or suggest a combination with Chehrazi and Diefendorff, and Diefendorff does not teach or suggest a combination with

Chehrazi and Mennemeier. Chehrazi teaches pipelining for a media processor. Mennemeir, in contrast, teaches sorting signed packed numbers. Diefendorff, in contrast to Mennemeier and Chehrazi, teaches executing of a graphics pixel packing instruction (Abstract). It would be impermissible hindsight, based on Applicants' own disclosure, to combine Chehrazi, Mennemeir, and Diefendorff.

Furthermore, even if Chehrazi, Mennemeier, and Diefendorff were combined, such a combination would lack selecting a first plurality of numbers from the first vector and a second plurality of numbers from the second vector according to a configuration specified by the instruction, as recited in amended claim 1.

Given that claims 4, 15, 29 and 39 contain related limitations, Applicants respectfully submit that claims 4, 15, 29 and 39 are not obvious under U.S.C. § 103(a) over Chehrazi in view of Mennemeier, and further in view of Diefendorff.

CONCLUSION

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

Blakely, Sokoloff, Taylor & Zafman, LLP

Date: October 30, 2006 By: _____

James C. Scheller
Reg. No.: 31,195

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(408) 720-8300